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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,564	12/11/2003	Robert W. Kooker	ANCO/55US1	8755

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EXAMINER	
VU, PHUONG T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 10/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,564	KOOKER ET AL.	
	Examiner	Art Unit	
	Phuong T. Vu	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18,23,24,26,33 and 36-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18,23,24,26,33 and 36-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2 Aug 04& 6 Apr 04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Regarding the information disclosure statement (IDS) submitted on April 6, 2004, the U.S. patent documents listed therein have been considered by the examiner. However, the foreign references and the International Search Report listed therein have not been considered, as these documents are not part of the application file. It is requested that Applicant submit a copy of each of these documents for consideration by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 18, 23-24, 33, 36-37, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Posner et al. (US 6,531,918B1) in view of Casebolt (US 5,774,344). Regarding claim 18, the Poser reference discloses an amplifier comprising a main amplifier subcircuit 14 and an error amplifier subcircuit 102. Poser provides a detailed discussion on the operation of subcircuits but is silent regarding any structural details of the amplifier including a circuit board upon which the subcircuits are positioned and a housing which receives the circuit board. It is required that the subcircuits be formed on a circuit board and necessary that the circuit board be provided with a housing to enclose the circuit board as well any other electronics to protect the entire assembly

from environmental conditions such as light, heat, moisture, dust, etc. which would damage the amplifier assembly. Furthermore, such a housing would provide mechanical support, some shock protection, and electromagnetic interference shielding. Casebolt discloses a known chassis body 10, a lid structure 24 for positioning with the chassis body to contain a single circuit board 32, the lid structure having side walls extending therefrom for defining a main cavity with subcavities to contain the subcircuits of the circuit, the sidewalls extending to contact the circuit board to isolate the subcircuits. The lid structure further including a dividing wall having multiple islands 30 extending therefrom, the multiple islands passing through multiple cut-outs formed in the circuit board between a main subcircuit and respective cavity and another subcircuit and respective cavity to electrically couple to the chassis body to separate the cavities and electrically isolate the main subcircuit and other subcircuits. The Casebolt reference is relied upon solely for this teaching. It would have been obvious to those skilled in the art at the time the invention was made to provide the amplifier subcircuits disclosed by Posner et al. with a circuit board 32 and a housing 10 as disclosed by Casebolt as recited for the above-mentioned advantages. In this configuration, an amplifier comprising a main amplifier subcircuit 14 and an error amplifier subcircuit 102 would be mounted on circuit board 32. A chassis body 10, a lid structure 24 for positioning with the chassis body contains the circuit board and therefore contains the main and error amplifier subcircuits. The lid structure 24 having side walls extending therefrom for defining a main cavity with subcavities to contain the subcircuits of the main amplifier subcircuit and an error amplifier cavity with subcavities to contain

subcircuits of the error amplifier subcircuit, the sidewalls extending to contact the circuit board to isolate the subcircuits. The lid structure further including a dividing wall having multiple islands 30 extending therefrom, the multiple islands passing through multiple cut-outs formed in the circuit board between a amplifier main subcircuit and respective cavity and the error amplifier subcircuit and respective cavity to electrically couple to the chassis body to separate the cavities and electrically isolate the main subcircuit and error amplifier subcircuits.

Regarding claim 23, the sidewalls are integrally formed with the lid structure.

Regarding claim 24, the sidewalls extend from the lid structure and further comprising additional subcircuits, the lid structure including at least one other sidewall extending from a side of the lid structure opposite the side wall extending from a side of the lid structure opposite the side wall for isolating subcircuits on both sides of the lid structure.

Regarding method claims 33, 36-37, one would necessarily perform the recited method steps in the assembly of the above-mentioned amplifier.

Regarding claim 39, please refer to the above rejection.

4. Claims 26, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Posner et al. (US 6,531,918B1) in view of Casebolt (US 5,774,344) and Jewell et al. (US 4,661,888). Regarding claim 26, neither Posner nor Casebolt discloses providing a gasket coupled between the sidewall and the circuit board for isolating the subcircuit. However, use of gaskets coupled between sidewalls and circuit boards is expedient in the art. Jewell discloses an electronic device comprising a chassis body 10 configured

for supporting subcircuits including amplifier subcircuits, a lid structure 12 for positioning with the chassis body over the subcircuits, the lid structure having sidewalls extending therefrom for surrounding a subcircuit and electrically isolating a subcircuit from the other subcircuits. Jewell discloses a gasket 25 coupled between the sidewall and the circuit board for electrically isolating the subcircuits. It would have been obvious to those skilled in the art at the time the invention was made to provide a gasket as taught by Jewell which is coupled between the sidewall and the circuit board for providing more efficient EMI shielding and isolation of the subcircuits.

Regarding method claim 38, one would necessarily perform the recited method steps in the assembly of the above-mentioned amplifier.

5. Claims 18, 23-24, 33, 36-37, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Powell et al. (US 4,612,512) in view of Casebolt (US 5,774,344). Regarding claim 18, the Powell reference discloses an amplifier comprising a main amplifier subcircuit 14 and an error amplifier subcircuit 50 mounted together on a single circuit board, a chassis body 80, a lid structure 72 for positioning with the chassis body to contain the circuit board and main and error amplifier subcircuits, the lid structure having side walls extending therefrom for defining a main cavity with subcavities to contain the subcircuits of the main amplifier subcircuit and an error amplifier cavity with subcavities to contain subcircuits of the error amplifier subcircuit, the sidewalls extending to contact the circuit board to isolate the subcircuits, the lid structure further including a dividing wall. Powell does not disclose that the dividing wall has multiple islands extending therefrom, the multiple islands passing through multiple cut-outs

formed in the circuit board between a amplifier main subcircuit and respective cavity and the error amplifier subcircuit and respective cavity to electrically couple to the chassis body to separate the cavities and electrically isolate the main subcircuit and error amplifier subcircuits. However Casebolt teaches providing a chassis body 10, a lid structure 24 for positioning with the chassis body to contain a circuit board and to necessarily contain the subcircuits formed on the single circuit board, the lid structure having side walls extending therefrom for defining a main cavity with subcavities to contain the subcircuits of the circuit, the sidewalls extending to contact the circuit board to isolate the subcircuits. The lid structure further including a dividing wall having multiple islands 30 extending therefrom, the multiple islands passing through multiple cut-outs formed in the circuit board between a main subcircuit and respective cavity and another subcircuit and respective cavity to electrically couple to the chassis body to separate the cavities and electrically isolate the main subcircuit and other subcircuits. It would have been obvious to those skilled in the art at the time the invention was made to provide multiple islands as disclosed by Casebolt in the assembly of Powell to provide a conductive path between the lid and chassis and the circuit card at the sidewalls to enhance internal and external RF shielding as taught by Casebolt.

Regarding claim 23, both Powell and Casebolt disclose that the sidewalls are integrally formed with the lid structure.

Regarding claim 24, both Powell and Casebolt disclose that the sidewalls extend from the lid structure and further comprising additional subcircuits, the lid structure including at least one other sidewall extending from a side of the lid structure opposite

the side wall extending from a side of the lid structure opposite the side wall for isolating subcircuits on both sides of the lid structure.

Regarding method claims 33, 36-37, one would necessarily perform the recited method steps in the assembly of the above-mentioned amplifier.

Regarding claim 39, please refer to the above rejection.

6. Claims 26, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Powell et al. (US 4,612,512) in view of Casebolt (US 5,774,344) and Jewell et al. (US 4,661,888). Regarding claim 26, neither Powell nor Casebolt discloses providing a gasket coupled between the sidewall and the circuit board for isolating the subcircuit. However, use of gaskets coupled between sidewalls and circuit boards is expedient in the art. Jewell discloses an electronic device comprising a chassis body 10 configured for supporting subcircuits including amplifier subcircuits, a lid structure 12 for positioning with the chassis body over the subcircuits, the lid structure having sidewalls extending therefrom for surrounding a subcircuit and electrically isolating a subcircuit from the other subcircuits. Jewell discloses a gasket coupled between the sidewall and the circuit board for electrically isolating the subcircuits. It would have been obvious to those skilled in the art at the time the invention was made to provide a gasket as taught by Jewell which is coupled between the sidewall and the circuit board for providing more efficient EMI shielding and isolation of the subcircuits.

Regarding method claim 38, one would necessarily perform the recited method steps in the assembly of the above-mentioned amplifier.

Response to Arguments

7. Applicant's arguments filed July 20, 2004 have been fully considered. The previous 35 U.S.C. 112 rejections have been withdrawn as claims 5-6 have been cancelled. The previous 35 U.S.C. 102 rejections have been withdrawn due to Applicant's amendments of the claims. Therefore, arguments regarding these rejections are moot.

Regarding the 35 U.S.C. 103 rejection based on Posner in view of Casebolt, Posner discloses an amplifier comprising a main amplifier and an error amplifier. Because Posner is directed only with the circuitry aspects of the amplifier and is silent about the incorporation of the circuitry into a physical structure comprising a housing element and a circuit board to support the circuitry, Casebolt was cited. As noted in the rejection, it is required that the amplifier circuitry be formed on a circuit board and necessary that the circuit board be provided with a housing to enclose the circuit board as well any other electronics to protect the entire assembly from environmental conditions such as light, heat, moisture, dust, etc. which would damage the amplifier assembly. Furthermore, such a housing would provide mechanical support, some shock protection, and electromagnetic interference shielding (which amplifier circuitry would require). However, Applicant states that Casebolt is directed to a box for shielding a circuit card. While this may be true, this housing or box supports a circuit card. The configuration of the housing and circuit board is designed to provide electromagnetic shielding and isolation between different subcircuits on a circuit board. The Casebolt reference is relied upon solely for this teaching of providing such shielding

and electrical isolation in a compact, efficient manner. Applicant further states that Casebolt fails to disclose an amplifier circuit nor discuss problems associated with amplifiers, which utilize two different amplifier subcircuits. However, as mentioned above, the Casebolt reference was not relied upon for the teaching of the amplifier. Posner was used to show the amplifier circuit. It is known that amplifier circuitry requires EMI shielding and that amplifier subcircuits, and any type of radio frequency circuitry and subcircuitry requires RF isolation (see Powell, Jewell, or Casebolt). Casebolt is relied upon for it's teaching of such a shielding housing with walls and islands for providing EMI shielding and RF isolation. Applicant further discusses the pins 30, which are disclosed by Casebolt and mentions that they are not the islands as disclosed in the invention. However, in response to these argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument that the examiner's conclusion of obviousness with the application of the Casebolt reference is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the

applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Finally, Applicant states that the present invention was a multiple tiered isolation scheme with an error amplifier and a main amplifier on the same circuit board, and that Posner and Casebolt do not teach this multiple tier isolation. It is noted that the present rejections fully address these issues. In the rejection based on Posner and Casebolt, Casebolt shows that the circuitry is provided on a single circuit board. Using more than one circuit board would provide no benefits and make the device less compact and more costly to manufacture. In the configuration taught by the combination of Posner and Casebolt, there would be no advantage to using multiple boards. A separate, alternative rejection based on Powell and Casebolt was also presented which discloses amplifier circuitry provided on a single board.

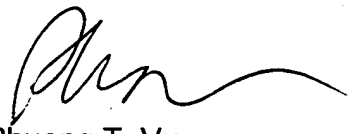
8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong T. Vu whose telephone number is (571) 272-2111. The examiner can normally be reached on Mon. & Tues., 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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